EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	20731	memory adj module	US-PGPUB; USPAT	OR	ON	2006/02/19 10:07
L2	11630	chip adj select	US-PGPUB; USPAT	OR	ON	2006/02/19 10:07
L3	1403	1 and 2	US-PGPUB; USPAT	OR	ON	2006/02/19 10:07
L4	109407	data adj transmission	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L5	215	3 and 4	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L6	50602	"365"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L7	62	5 and 6	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L8	17	park-myun-joo.in.	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L9	42	so-byung-se.in.	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08
L10	21	lee-jae-jun.in.	US-PGPUB; USPAT	OR	ON	2006/02/19 10:08

Day : Sunday
Date: 2/19/2006

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Time: 10:10:06

Inventor Name Search Result

Your Search was:

Last Name = PARK
First Name = MYUN-JOO

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09777446	6772262	150	02/06/2001	MEMORY MODULE WITH IMPROVED DATA BUS PERFORMANCE	PARK, MYUN-JOO
09777547	6414904	150	02/06/2001	TWO CHANNEL MEMORY SYSTEM HAVING SHARED CONTROL AND ADDRESS BUS AND MEMORY MODULES USED THEREFOR	PARK, MYUN-JOO
09851277	Not Issued	71	05/08/2001	Memory interface systems that couple a memory to a memory controller and are responsive to a terminal voltage that is independent of supply voltages for the memory and the memory controller	PARK, MYUN-JOO
09858401	6480409	150	05/16/2001	MEMORY MODULES HAVING INTEGRAL TERMINATING RESISTORS AND COMPUTER SYSTEM BOARDS FOR USE WITH SAME	PARK, MYUN-JOO
10200731	6870742	150	07/22/2002	SYSTEM BOARD	PARK, MYUN-JOO
10353924	6828819	150	01/30/2003	HIGH-SPEED MEMORY SYSTEM	PARK, MYUN-JOO
10424923	Not Issued	41	04/29/2003	Semiconductor memory device with data bus scheme for reducing high frequency noise	PARK, MYUN-JOO
10629866	Not Issued	71	07/30/2003	Memory system having memory modules with different memory device loads	PARK, MYUN-JOO
10644735	Not Issued	71	08/21/2003	Semiconductor memory system having multiple system data buses	PARK, MYUN-JOO

10883488	6990543	150	07/01/2004	MEMORY MODULE WITH IMPROVED DATA BUS PERFORMANCE	PARK, MYUN-JOO

Inventor Search Completed: No Records to Display.

Search Another: Inventor **Last Name** park **First Name** myun-joo Search

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Inventor Name Search Result

Your Search was:

Last Name = SO
First Name = BYUNG-SE

Application#	Patent#	Status	Date Filed	Title	Inventor Name
08773787	5856982	150	12/24/1996	HIGH-SPEED DISTURB TESTING METHOD AND WORD LINE DECODER IN SEMICONDUCTOR MEMORY DEVICE	SO, BYUNG-SE
09426609	6714595	150	10/26/1999	SIGNAL TRANSMISSION CIRCUITS THAT USE MULTIPLE INPUT SIGNALS TO GENERATE A RESPECTIVE TRANSMIT SIGNAL AND METHODS OF OPERATING THE SAME	SO, BYUNG-SE
09454339	6587976	150	12/03/1999	SEMICONDUCTOR DEVICE TESTER FOR MEASURING SKEW BETWEEN OUTPUT PINS OF A SEMICONDUCTOR DEVICE	SO, BYUNG-SE
09540988	6252805	150	03/31/2000	Semiconductor memory device including programmable output pin determining unit and method of reading the same during test mode	SO, BYUNG-SE
09612610	6382986	150	07/08/2000	Socket for mounting memory module boards on a printed circuit board	SO, BYUNG-SE
09688297	6632705	150	10/13/2000	MEMORY MODULES AND PACKAGES USING DIFFERENT ORIENTATIONS AND TERMINAL ASSIGNMENTS	SO, BYUNG-SE
09777446	6772262	150	02/06/2001	MEMORY MODULE WITH IMPROVED DATA BUS PERFORMANCE	SO, BYUNG-SE
09777547	6414904	150	02/06/2001	TWO CHANNEL MEMORY	SO, BYUNG-SE

				SYSTEM HAVING SHARED CONTROL AND ADDRESS BUS AND MEMORY MODULES USED THEREFOR	
09851277	Not Issued	71	05/08/2001	Memory interface systems that couple a memory to a memory controller and are responsive to a terminal voltage that is independent of supply voltages for the memory and the memory controller	SO, BYUNG-SE
09858401	6480409	150	05/16/2001	MEMORY MODULES HAVING INTEGRAL TERMINATING RESISTORS AND COMPUTER SYSTEM BOARDS FOR USE WITH SAME	SO, BYUNG-SE
10043047	Not Issued	61	01/09/2002	Memory system having stub bus configuration	SO, BYUNG-SE
10074309	6754112	150	02/11/2002	INTEGRATED CIRCUIT DEVICES HAVING DELAY CIRCUITS FOR CONTROLLING SETUP/DELAY TIMES OF DATA SIGNALS THAT ARE PROVIDED TO MEMORY DEVICES AND METHODS OF OPERATING SAME	SO, BYUNG-SE
10094448	6944737	150	03/08/2002	MEMORY MODULES AND METHODS HAVING A BUFFER CLOCK THAT OPERATES AT DIFFERENT CLOCK FREQUENCIES ACCORDING TO THE OPERATING MODE	SO, BYUNG-SE
10200731	6870742	150	07/22/2002	SYSTEM BOARD	SO, BYUNG-SE
10353924	6828819	150	01/30/2003	HIGH-SPEED MEMORY SYSTEM	SO, BYUNG-SE
10629866	Not Issued	71	07/30/2003	Memory system having memory modules with different memory device loads	SO, BYUNG-SE
10644735	Not Issued	71	08/21/2003	Semiconductor memory system having multiple system data buses	SO, BYUNG-SE
10722159	Not Issued	61	11/26/2003	Multi-chip package for reducing parasitic load of pin	SO, BYUNG-SE
10794680	Not Issued	93	03/05/2004	SIGNAL TRANSMISSION CIRCUITS THAT USE	SO, BYUNG-SE

				MULTIPLE INPUT SIGNALS TO GENERATE A RESPECTIVE TRANSMIT SIGNAL	
10795507	6836138	150	03/09/2004	MODULE HAVING TEST ARCHITECTURE FOR FACILITATING THE TESTING OF BALL GRID ARRAY PACKAGES, AND TEST METHOD USING THE SAME	SO, BYUNG-SE
10831702	Not Issued	30	04/23/2004	Memory module and method of testing the same	SO, BYUNG-SE
10833322	Not Issued	30	04/28/2004	Buffered memory module and method for testing same	SO, BYUNG-SE
10837610	Not Issued	71	05/04/2004	Memory system with improved signal integrity	SO, BYUNG-SE
10853353	Not Issued	93	05/26/2004	MEMORY MODULE	SO, BYUNG-SE
10883488	6990543	150	07/01/2004	MEMORY MODULE WITH IMPROVED DATA BUS PERFORMANCE	SO, BYUNG-SE
10900140	Not Issued	30	07/28/2004	Memory module test system	SO, BYUNG-SE
10913359	Not Issued	30	08/09/2004	Data transmission system and method	SO, BYUNG-SE
10975810	Not Issued	20	10/27/2004	Memory module with registers	SO, BYUNG-SE
10988390	Not Issued	41	11/12/2004	Mounting structure in integrated circuit module	SO, BYUNG-SE
10997406	Not Issued	30	11/24/2004	Memory module system with efficient control of on-die termination	SO, BYUNG-SE
11029008	Not Issued	41	01/05/2005	Memory module, memory unit, and hub with non-periodic clock and methods of using the same	SO, BYUNG-SE
11064671	Not Issued	30	02/24/2005	Memory module and a method of arranging a signal line of the same	SO, BYUNG-SE
11102181	Not Issued	30	04/08/2005	Memory module with memory devices of different capacity	SO, BYUNG-SE
11118377	Not Issued	20	05/02/2005	Method of testing a memory module and hub of the memory module	SO, BYUNG-SE
11177736	Not Issued	30	07/08/2005	Stacked board-on-chip package having mirroring structure and dual inline memory module on	SO, BYUNG-SE

				which the stacked board-on-chip package are mounted	
11181059	Not Issued	30	07/13/2005	Error detecting memory module and method	SO, BYUNG-SE
11227225	Not Issued	30	09/16/2005	Method of testing memory module and memory module	SO, BYUNG-SE
11256580	Not Issued	20	10/21/2005	Determining operation mode for semiconductor memory device	SO, BYUNG-SE
11266428	Not Issued	30	11/04/2005	Memory module with stacked semiconductor devices	SO, BYUNG-SE
60267908	Not Issued	159	02/09/2001	Memory system having stub bus configuration	SO, BYUNG-SE
60579657	Not Issued	159	06/16/2004	Method of testing memory module in transparent mode and hub of memory module of testing the same	SO, BYUNG-SE
10455434	Not Issued	71	06/06/2003	Method of and apparatus for inputting character using pointing device	SOH, BYUNG-SEOK
10735906	Not Issued	41	12/16/2003	Apparatus and method for detecting finger-motion	SOH, BYUNG-SEOK
11043423	Not Issued	30	01/27/2005	Method of adjusting pointing position during click operation and 3D input device using the same	SOH, BYUNG-SEOK
11183171	Not Issued	20	07/18/2005	Apparatus and method for providing haptics of image	SOH, BYUNG-SEOK
11285191	Not Issued	19	11/23/2005	Key input apparatus using magnetic force, operating method thereof, and computer-readable recording medium storing computer programs for performing the method	SOH, BYUNG-SEOK
08965570	Not Issued	161	11/06/1997	SENSE AMPLIFIER HAVING SELF-ADJUSTING PULL-UP CIRCUIT	SOHN, BYUNG-SEH

Inventor Search Completed: No Records to Display.

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Inventor Name Search Result

Your Search was:

Last Name = LEE
First Name = JAE-JUN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09226130	6333762	150	01/07/1999	METHOD FOR MAKING LOOK-UP TABLES FOR VIDEO FORMAT CONVERTER USING THE LOOK-UP TABLES	LEE, JAE-JUN
09790632	6607867	150	02/23/2001	ORGANOMETAL-CONTAINING NORBORNENE MONOMER, PHOTORESIST CONTAINING ITS POLYMER, MANUFACTURING METHOD THEREOF, AND METHOD OF FORMING PHOTORESIST PATTERNS	LEE, JAE-JUN
10200731	6870742	150	07/22/2002	SYSTEM BOARD	LEE, JAE-JUN
10424923	Not Issued	41	04/29/2003	Semiconductor memory device with data bus scheme for reducing high frequency noise	LEE, JAE-JUN
10629866	Not Issued	71	07/30/2003	Memory system having memory modules with different memory device loads	LEE, JAE-JUN
10644735	Not Issued	71	08/21/2003	Semiconductor memory system having multiple system data buses	LEE, JAE-JUN
10784806	6936402	150	02/24/2004	NOVEL MONOMERS CONTAINING AN OXEPAN-2-ONE GROUP, PHOTORESIST COMPOSITIONS COMPRISING POLYMERS PREPARED FROM THE MONOMERS, METHODS FOR PREPARING THE COMPOSITIONS, AND METHODS FOR FORMING PHOTORESIST PATTERNS USING THE COMPOSITIONS	LEE, JAE-JUN
10833322	Not	30	04/28/2004	Buffered memory module and	LEE, JAE-JUN

	Issued			method for testing same	
10837610	Not Issued	71	05/04/2004	Memory system with improved signal integrity	LEE, JAE-JUN
10853353	Not Issued	93	05/26/2004	MEMORY MODULE	LEE, JAE-JUN
10913359	Not Issued	30	08/09/2004	Data transmission system and method	LEE, JAE-JUN
10997406	Not Issued	30	11/24/2004	Memory module system with efficient control of on-die termination	LEE, JAE-JUN
11064671	Not Issued	30	02/24/2005	Memory module and a method of arranging a signal line of the same	LEE, JAE-JUN
11221301	Not Issued	20	09/06/2005	Method for providing mobile service using code-pattern	LEE, JAE-JUN
11247846	Not Issued	30	10/11/2005	Impedance adjustment circuits and methods using replicas of variable impedance circuits	LEE, JAE-JUN
11321599	Not Issued	20	12/29/2005	Delay locked loop circuit for a synchronous semiconductor memory device and a method of generating information about a load connected to a data pin of a synchronous semiconductor memory device	LEE, JAE-JUN

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